# C2DTUDCOMR01 – CFP2 Dual Fibre DWDM

## DWDM Tunable 50GHz / Coherent / 100GBASE & OTU4

*For your product safety, please read the following information carefully before any manipulation of the transceiver:*

*ESD*

*This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.*

*LASER SAFETY*

*This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).*

*The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.*

## 1. Overview

C2DTUDCOMR01 is a high performance CFP2 transceiver module for 100Gbps DP-QPSK modulated or 200Gbps DP-8/16QAM modulated data links over two single mode fibres. The maximum reach is beyond 2000km without inline chromatic dispersion compensation. The amplified narrow linewidth tunable laser is shared between the transmitter and receiver sections. A tapped monitor diode is used to control the optical output power.
The receiver module is performing the coherent intradyne reception and O/E conversion of the incoming optical signal after being mixed with a local optical oscillator. Four pairs of balanced photo detectors perform quadratic detection and produce I and Q components of the two orthogonal polarizations (H and V).
This transceiver module is compliant with the CFP Multisource Agreement (MSA) and hot pluggable. Always contact Skylane Optics commercial agents for compatibility with different equipment platforms.

## 2. Features

- CFP Multi-Source Agreement compliant
- Hot pluggable CFP2 footprint
- Supports CAUI-4 for 100GE and CEI-28G-VSR for OTU4 Host Interface
- Proprietary Internal Soft-Decision Forward Error Correction (SD-FEC)
- Supports Host and Line-Side Loopback
- Tunable C-band Transmitter
- Coherent Receiver
- Beyond 1000/2000km reach on Single Mode Fibre
- Operating temperature range 0°C to 70°C
- Power Consumption < 19W
- Single +3.3V Power Supply
- MDIO Management Interface

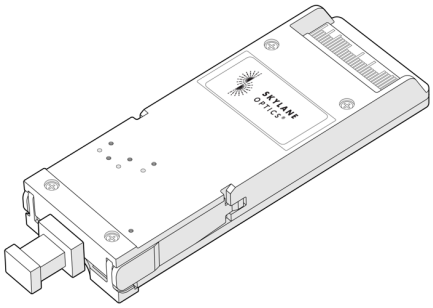

Figure 1. CFP2 Dual Fibre
(non-binding illustration)

## 3. Applications

- 1× IEEE 100GBASE or ITU-T OTU4
- 2× IEEE 100GBASE or ITU-T OTU4 or mix (MUXPONDER)

## 4. Optical Interface

| P/N | Wavelength | Protocol | Optical Output Power[1] [dBm] | Optical Receiver Sensitivity[2] [dBm] | Optical Receiver Overload[3] [dBm] |
|---|---|---|---|---|---|
| **C2DTUDCOMR01** | ITU DWDM | 100GBASE OTU4 | -15 to 1 | ≤ -25 | 0 |

1. EOL over operating temperature range, settable in steps of 0.1dB
2. See section 5.4 for definitions
3. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers (optical loop back) before ensuring that proper optical attenuation is used

## 5. Technical Parameters

### 5.1. Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Storage temperature | -40 | | 85 | °C | |
| Operating Case Temperature | 0 | | 70 | °C | |
| Relative Humidity | | | 85 | % | Non-Condensing |
| Power Supply Voltage | 3.2 | 3.3 | 3.4 | V | |
| Power Supply Current | | | 6 | A | |
| Power Dissipation | | | 19 | W | |

### 5.2. General Specifications

| Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supported Host Signal Types | | 103.125 | | Gbps | 4 |
| | | 111.81 | | | 5 |

4. 100GE as per IEEE 802.3ba. The line format can be selected as OTU4 (G.709 HD-FEC) or with SD-FEC (proprietary)
5. OTU4 as per ITU-T G.709. The line format can be selected as OTU4 (transparent) or with S-DFEC (proprietary)

### 5.3. Transmitter Optical Specifications

| Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Average Output Power | -15 | | 1 | dBm | 6, 7 |
| Output Power Accuracy and Stability | -1 | | 1 | dB | 7, 8 |
| Centre Wavelength Range | 1528.77 | | 1567.54 | nm | |
| Frequency Grid Setting | | 50 | | GHz | 9 |
| Centre Wavelength | $\lambda_T$ -15 | $\lambda_T$ | $\lambda_T$ +15 | pm | 9 |

6. The output power is settable in steps of 0.1 dB within the specified wavelength range
7. Output power coupled into a 9/125 µm single mode fibre
8. Difference between the set value and actual value
9. Per ITU-T G.694.1 grid definition

### 5.4. Receiver Optical Specifications

| Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Receiver Operating Wavelength | 1528.77 | | 1567.54 | nm | |
| Receiver Input Power Range | -18 | | 0 | dBm | 10 |
| Receiver Sensitivity | | | -25 | dBm | 11 |
| OSNR Tolerance | | 11.5 | | dB/0.1nm | 12, 13 |
| | | 17 | | | 12, 14 |
| | | 20 | | | 12, 15 |
| Chromatic Dispersion Tolerance | | | 40 | ns/nm | 13 |
| | | | 20 | | 14, 15 |

10. An input power in this range guarantees optimum OSNR performance
11. Minimum input power needed to achieve post-FEC BER ≤ $10^{-15}$ (OSNR > 35dB, SD-FEC enabled)
12. Post-FEC BER ≤ $10^{-15}$, SD-FEC enabled
13. 100G QPSK, post-FEC BER ≤ $10^{-15}$, SD-FEC enabled
14. 200G 8QAM, post-FEC BER ≤ $10^{-15}$, SD-FEC enabled
15. 200G 16QAM, post-FEC BER ≤ $10^{-15}$, SD-FEC enabled

## 6. Transceiver Electrical Pad Layout

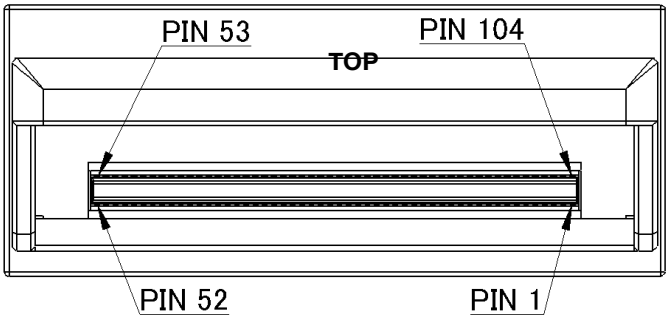


Figure 2. Transceiver Electrical Pad Layout

## 7. Module Electrical Pin Definition

| Pin | Symbol | I/O | Description | Logic | Pin | Symbol | I/O | Description | Logic |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | | Ground | | 53 | GND | | Ground | |
| 2 | OHIO_RDn | O | Overhead extraction | | 54 | RX7p | O | Ch7 25Gbps Receive Output | CML |
| 3 | OHIO_RDp | | | | 55 | RX7n | | | |
| 4 | GND | | Ground | | 56 | GND | | Ground | |
| 5 | OHIO_TDn | I | Overhead insertion | | 57 | RX0p | O | Ch0 25Gbps Receive Output | CML |
| 6 | OHIO_TDp | | | | 58 | RX0n | | | |
| 7 | 3.3V_GND | | Ground | | 59 | GND | | Ground | |
| 8 | 3.3V_GND | | | | 60 | RX1p | O | Ch1 25Gbps Receive Output | CML |
| 9 | 3.3V | | 3.3V Power Supply | | 61 | RX1n | | | |
| 10 | 3.3V | | | | 62 | GND | | Ground | |
| 11 | 3.3V | | | | 63 | RX6p | O | Ch6 25Gbps Receive Output | CML |
| 12 | 3.3V | | | | 64 | RX6n | | | |
| 13 | 3.3V_GND | | Ground | | 65 | GND | | Ground | |
| 14 | 3.3V_GND | | | | 66 | RX5p | O | Ch5 25Gbps Receive Output | CML |
| 15 | VND_IO_A | | Do not connect | | 67 | RX5n | | | |
| 16 | VND_IO_B | | | | 68 | GND | | Ground | |
| 17 | PRG_CNTL1 | I | Programmable Control 1 | LVCMOS w/ PUR | 69 | RX2p | O | Ch2 25Gbps Receive Output | CML |
| 18 | PRG_CNTL2 | | Programmable Control 2 | | 70 | RX2n | | | |
| 19 | PRG_CNTL3 | | Programmable Control 3 | | 71 | GND | | Ground | |
| 20 | PRG_ALRM1 | O | Programmable Alarm 1 | LVCMOS | 72 | RX3p | O | Ch3 25Gbps Receive Output | CML |
| 21 | PRG_ALRM2 | | Programmable Alarm 2 | | 73 | RX3n | | | |
| 22 | PRG_ALRM3 | | Programmable Alarm 3 | | 74 | GND | | Ground | |
| 23 | GND | | Ground | | 75 | RX4p | O | Ch4 25Gbps Receive Output | CML |
| 24 | TX_DIS | I | Transmitter Disable | LVCMOS w/ PUR | 76 | RX4n | | | |
| 25 | RX_LOS | O | Loss of Optical Input Signal | LVCMOS | 77 | GND | | Ground | |
| 26 | MOD_LOPWR | I | Module Low Power Mode | LVCMOS w/ PUR | 78 | REFCLKp | | Not Used | |
| 27 | MOD_ABS | O | Module Absent Indicator | GND | 79 | REFCLKn | | | |
| 28 | MOD_RSTn | I | Module Reset | LVCMOS w/ PDR | 80 | GND | | Ground | |
| 29 | GLB_ALRMn | O | Global Alarm | LVCMOS (open drain) | 81 | TX7p | I | Ch7 25Gbps Transmit Input | CML |
| 30 | GND | | Ground | | 82 | TX7n | | | |
| 31 | MDC | I | Management Data Clock | 1.2V CMOS | 83 | GND | | Ground | |
| 32 | MDIO | I/O | Management bi-dir. Data | 1.2V CMOS | 84 | TX0p | I | Ch0 25Gbps Transmit Input | CML |
| 33 | PRTADR0 | I | MDIO Physical Port addr. bit0 | 1.2V CMOS | 85 | TX0n | | | |
| 34 | PRTADR1 | | MDIO Physical Port addr. bit1 | | 86 | GND | | Ground | |
| 35 | PRTADR2 | | MDIO Physical Port addr. bit2 | | 87 | TX1p | I | Ch1 25Gbps Transmit Input | CML |
| 36 | VND_IO_C | | Do not connect | | 88 | TX1n | | | |
| 37 | VND_IO_D | | | | 89 | GND | | Ground | |
| 38 | VND_IO_E | | | | 90 | TX6p | I | Ch6 25Gbps Transmit Input | CML |
| 39 | 3.3V_GND | | Ground | | 91 | TX6n | | | |
| 40 | 3.3V_GND | | Ground | | 92 | GND | | Ground | |
| 41 | 3.3V | | 3.3V Power Supply | | 93 | TX5p | I | | CML |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 42 | 3.3V | | | | 94 | TX5n | | Ch5 25Gbps Transmit Input | |
| 43 | 3.3V | | | | 95 | GND | | Ground | |
| 44 | 3.3V | | | | 96 | TX2p | I | Ch2 25Gbps Transmit Input | CML |
| 45 | 3.3V_GND | | Ground | | 97 | TX2n | | | |
| 46 | 3.3V_GND | | | | 98 | GND | | Ground | |
| 47 | OHIO_REFCLKn | I | Overhead I/O Reference Clock | | 99 | TX3p | I | Ch3 25Gbps Transmit Input | CML |
| 48 | OHIO_REFCLKp | | | | 100 | TX3n | | | |
| 49 | GND | | Ground | | 101 | GND | | Ground | |
| 50 | RX_MCLKn | | Not for normal use | | 102 | TX4p | I | Ch4 25Gbps Transmit Input | CML |
| 51 | RX_MCLKp | | | | 103 | TX4n | | | |
| 52 | GND | | Ground | | 104 | GND | | Ground | |

## 8. Register Allocation

The total CFP register space (from 8000h to FFFFh) is logically divided into 8 pages with each page starting at even hex thousand, that is, 8000h, 9000h, A000h, …, F000h, with each page further divided into 32 tables.
The CFP MSA specifies the starting address of all non-volatile registers (NVR) at 8000h (8 NVR tables in total).
Page A000h is allocated for volatile registers (VR). The CFP MSA specifies four VR tables for module configuration, control, and various DDM related functions.

| Start Address (hex) | End Address (hex) | Table Name and Description |
|---|---|---|
| 0000 | 7FFF | Reserved for IEEE 802.3 use |
| 8000 | 807F | CFP NVR 1. Basic ID registers |
| 8080 | 80FF | CFP NVR 2. Extended ID registers |
| 8100 | 817F | CFP NVR 3. Network lane specific registers |
| 8180 | 81FF | CFP NVR 4 |
| 8200 | 83FF | MSA Reserved |
| 8400 | 847F | Vendor NVR 1. Vendor data registers |
| 8480 | 84FF | Vendor NVR 2. Vendor data registers |
| 8500 | 87FF | Reserved by CFP MSA |
| 8800 | 887F | User NVR 1. User data registers |
| 8880 | 88FF | User NVR 2. User data registers |
| 8900 | 8EFF | Reserved by CFP MSA |
| 8F00 | 8FFF | Reserved for User private use |
| 9000 | 9FFF | Reserved for vendor private use |
| A000 | A07F | CFP Module VR 1. CFP Module level control and DDM registers |
| A080 | A0FF | MLG VR 1. MLG Management Interface registers |
| A100 | A1FF | Reserved by CFP MSA |
| A200 | A27F | Network Lane VR 1. Network lane specific registers |
| A280 | A2FF | Network Lane VR 2. Network lane specific registers |
| A300 | A37F | Network Lane VR 3. Network Lane n Vendor Specific FAWS Registers |
| A380 | A3FF | Reserved by CFP MSA |
| A400 | A47F | Host Lane VR 1. Host lane specific registers |
| A480 | ABFF | Reserved by CFP MSA |
| AC00 | AFFF | Common Data Block Registers |
| B000 | BFFF | Allocated for OIF MSA-100GLH modules |
| C000 | FFFF | Reserved by CFP MSA |

Figure 3. Register of a CFPx

## 9. Ordering Information

| Part Number | Description |
|---|---|
| **C2DTUDCOMR01** | CFP2 DCO, DWDM, Tx (tunable), Rx (coherent), 1000km/2000km reach on SMF,<br>100G/200G (one or two clients) 100Gigabit Ethernet & OTU4, dual LC connector, 0°C to 70°C, DDM |

## 10. Document Revision Information

| Revision | Description |
|---|---|
| **A** | Initial release |

Skylane Optics supplies a broad range of optical transceivers. Our engineers work closely with our customers to find the best solutions for every application. We are committed to provide high quality products and services to our customers.

For questions on this product please contact:
**support@skylaneoptics.com**